CLAIMS

What is claimed is:

1. A thin film transistor, comprising:

an active layer formed on an insulating substrate and having channel, source, and drain regions formed therein;

wherein a voltage is applied to the channel region to discharge hot carriers generated in the channel region.

2. The thin film transistor according to claim 1, wherein the voltage applied to the channel region is equal to a voltage applied to the source or drain region.

3. The thin film transistor according to claim 1, wherein the active layer further comprises a bias supply layer contacted with the channel region and separated from the source and drain regions, wherein the voltage applied to the channel region is directly applied to the bias supply layer.

4. The thin film transistor according to claim 3, wherein a conductivity type of the bias supply layer is different from a conductivity type of the source and drain regions, and the voltage applied to the bias supply layer is equal to a voltage applied to the source or drain region.

5. The thin film transistor according to claim 1, wherein the active layer further comprises:

a bias supply layer contacted with the channel region and separated from the source and drain regions; and

a contact wiring connected to the bias supply layer to apply the voltage to the channel region through the bias supply layer,

wherein the voltage applied to the channel region is directly applied to the bias supply layer through the contact wiring.

6. The thin film transistor according to claim 5, wherein a conductivity type of the bias supply layer is different from a conductivity type of the source and drain regions, and the voltage applied to the bias supply layer is equal to a voltage applied to the source or drain region.

7. A thin film transistor, comprising:

an active layer formed on an insulating substrate and having channel, source, and drain regions formed therein;

a gate electrode formed over the channel region of the active layer;

source and drain electrodes respectively formed over the source and drain regions of the active layer; and

a body contact region formed in the active layer so that the body contact region is contacted with the channel region and separated from the source and drain regions,

wherein a voltage is applied to the channel region through the body contact region.

8. The thin film transistor according to claim 7, wherein the body contact region is directly connected to the source electrode or drain electrode so that the voltage applied to the channel region is equal to a voltage applied to the source or drain electrode.

9. The thin film transistor according to claim 8, wherein the source and drain regions and the body contact region are impurity regions, and the channel region is an intrinsic region.

10. The thin film transistor according to claim 9, wherein a conductivity type of the body contact region is different from a conductivity type of the source and drain regions.

11. The thin film transistor according to claim 7, wherein the thin film transistor further comprises a contact wiring connecting the body contact region to the source electrode or drain electrode.

12. The thin film transistor according to claim 11, wherein the voltage applied to the channel region through the body contact region is equal to a voltage applied to the source or drain electrode, and is applied though the contact wiring to the body contact region.

13. The thin film transistor according to claim 11, wherein the source and drain regions and the body contact region are impurity regions, and the channel region is an intrinsic region.

14. The thin film transistor according to claim 13, wherein a conductivity type of the body contact region is different from a conductivity type of the source and drain regions.

15. The thin film transistor according to claim 7, wherein the thin film transistor further comprises:

a contact wiring connected to the body contact region; and

a connect wiring connecting the contact wiring to the source electrode or drain electrode;

wherein the voltage applied to the channel region through the body contact region is equal to a voltage supplied from the source or drain electrode through the connect wiring to the contact wiring.

16. A flat panel display comprising:

a gate line, a data line and a power supply line; and

a plurality of pixels connected to the lines;

wherein each of the pixels comprises one or more thin film transistors comprising channel, source, and drain regions in an active layer, and a voltage is applied to the channel region of the thin film transistor to discharge hot carriers.

17. The flat panel display according to claim 16, wherein the thin film transistor further comprises:

a bias supply layer formed in the active layer so that the bias supply layer is contacted with the channel region and separated from the source and drain regions; and

a contact wiring connected to the bias supply layer to apply the voltage to the channel region.

18. The flat panel display according to claim 16, wherein a conductivity type of the bias supply layer is different from a conductivity type of the source and drain regions.

19. The flat panel display according to claim 17, wherein the bias supply layer is connected to the data line or power supply line though the contact wiring.

20. A flat panel display comprising:

a plurality of pixels arranged in a matrix shape, each of the pixels comprising at least one thin film transistor,

wherein the at least one thin film transistor in each of the pixels comprises:

an active layer having channel, source, and drain regions formed therein, and

source and drain electrodes connected to the source and drain regions, respectively;

wherein the active layer further comprises a bias supply layer to supply a bias voltage to the channel region.

21. The flat panel display according to claim 20, wherein the bias supply layer is directly connected to the source electrode or drain electrode, and the bias voltage is directly applied to the bias supply layer from the source or drain electrode.

22. The flat panel display according to claim 20, wherein the thin film transistor further comprises a contact wiring connecting the bias supply layer to the source electrode or drain electrode, and the bias voltage is applied to the bias supply layer through the contact wiring from the source or drain electrode.

23. The flat panel display according to claim 20, wherein the bias supply layer is an impurity region contacted with the channel region and separated from the source and drain regions.

24. The flat panel display according to claim 20, wherein the bias supply layer is a region on which impurities having a conductivity type different from the source/drain regions are doped, and the channel region is an intrinsic region.

25. A method of fabricating a thin film transistor comprising:

forming an active layer on an insulating substrate;

forming a gate insulation film on the insulating substrate;

forming source, drain, and body contact regions which are separated by a channel region in the active layer;

forming a gate on the gate insulation film;

forming an interlayer insulation film on the insulating substrate; and

forming source and drain electrodes electrically connected with the source and drain regions, respectively,

wherein a voltage is applied to the channel region of the active layer through the body contact region.

26. The method of fabricating a thin film transistor according to claim 25, wherein the body contact region is directly connected to the source or drain electrode, and the voltage is directly applied to the body contact region from the source or drain electrode.

27. The method of fabricating a thin film transistor according to claim 25, further comprising forming a contact wiring, electrically connected to the body contact region, at the same time of the forming of the source and drain electrodes.

28. The method of fabricating a thin film transistor according to claim 27, wherein the body contact region is connected to the source or drain electrode through the contact wiring, and the voltage is applied to the body contact region through the contact wiring from the source or drain electrode.

29. The method of fabricating a thin film transistor according to claim 25, wherein the forming of the source, drain, and body contact regions and the forming of the gate comprises:

forming the body contact region by ion implanting impurities of a first conductivity type into the active layer using a first photosensitive film pattern;

forming a gate electrode on the gate insulation film; and

forming the source and drain regions by ion implanting impurities of a second conductivity type into the active layer using a second photosensitive film pattern and the gate electrode as a mask;

wherein a portion on which impurities of the first and second conductivity types are not doped in the active layer functions as the channel region, and the channel region is contacted with the source and drain regions and the body contact region so that the source, drain, and body contact regions are separated by the channel region.

30. The method of fabricating a thin film transistor according to claim 25, wherein the forming of the source, drain, and body contact regions and the forming of the gate comprises:

forming a gate electrode;

forming the source and drain regions by ion implanting impurities of a first conductivity type into the active layer using first photosensitive film pattern and the gate electrode as a mask; and

forming the body contact region by ion implanting impurities of a second conductivity type into the active layer using a second photosensitive film pattern,

wherein a portion on which impurities of the first and second conductivity types are not doped in the active layer functions as the channel region, and the channel region is contacted with the source and drain regions and the body contact region so that the source, drain, and body contact regions are separated by the channel region.

31. An active layer of a thin film transistor, the active layer comprising:

a source region;

a drain region;

a channel region; and

a bias supply region to supply a voltage to the channel region to discharge hot carriers.

32. The active layer of claim 31, wherein the bias supply region is connected to the source or drain region.

33. A thin film transistor, wherein a voltage is applied to a channel region by a member other than a gate electrode, and wherein the voltage discharges hot carriers generated in the channel region.